DUAL-GAIN LOOP CIRCUITRY
FOR PROGRAMMABLE LOGIC DEVICE

Abstract of the Disclosure

[0068] A loop circuit (PLL or DLL) uses a dual-gain voltage-controlled component (VCO or VCDL) to achieve a phase (and frequency) lock with reduced jitter. A coarse control feedback path includes a detector for achieving an approximate lock. This path operates over a wide range and therefore feeds a VCO or VCDL input with relatively high gain. However, input on that path is fixed once coarse frequency lock is achieved, so it does not contribute to jitter. A fine control path includes a detector whose output fine tunes the lock. Although this path is susceptible to noise, its operating range is relatively small, so its VCO or VCDL input has relatively low gain. Therefore jitter from magnification of noise by that gain is relatively small. The loop circuit can be used in a programmable logic device, in which case various loop parameters may be determined by programmable values.